1. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit streams of data;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output and including

a writeable instruction memory containing instructions; and

a receive processor that sequentially executes certain of the instructions to process the data stream received from the data stream input and/or

a transmit processor that sequentially executes certain of the instructions to process the data stream for output to the data stream output.

2. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit data streams;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output and including

a writeable local memory local to the data stream processor,

the plurality of local memories belonging to a global address space which is addressable by any of the data stream processors.

3. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit data streams;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output; and

a context processor that responds to information received from a given data stream processor that is processing a data stream to produce information about the given data stream's context and provide the context information to the processor;

the given data stream processor using the context information to process the data stream.

4. The integrated circuit set forth in claim 3 wherein:

the context processor receives the information and provides the context information by means of a bus on which there is an upper bound for latency for each of the data stream processors and the context processor.

5. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit data streams, a data stream containing control data and a payload;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output, a received data stream being processed to extract the control data and the payload and a transmitted data stream being processed to add control data to the payload;

a buffer manager that provides addresses of buffers for storing payload and responds to a write operation with a buffer address to write payload to the addressed buffer and to a read operation with a buffer address to read payload from the addressed buffer; and

a queue manager that manages queues of descriptors of payload, each descriptor including at least a buffer address, the queue manager responding to an enqueue command by enqueuing a descriptor provided with the command to a queue specified in the command and responding to a dequeue command by dequeuing a descriptor from the queue specified in the command,

a data stream processor responding to a received data stream by performing a write operation to the buffer manager with the received data stream's payload and an address provided by the buffer manager and performing an enqueue operation with a descriptor containing the address and transmitting a data stream by performing a dequeue operation, using the address in a descriptor obtained as a result of the dequeue operation in a read operation to the buffer manager, producing a data stream using the payload received from the buffer manager, and transmitting the produced data stream.

6. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit data streams;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output; and

an aggregator that aggregates certain of the data stream processors so that the aggregated data stream processors cooperate in processing a data stream, the aggregator including

configurable interconnections between the aggregated data stream processors;

a configurable operation coordinator that coordinates operation of the aggregated data stream processors; and

a configurator that specifies the configurable interconnections and the configurable operation coordinator as required to aggregate the data stream processors.

7. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit data streams;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output and including

a control data processor,

a receive processor that processes data streams received from the data stream input and/or

a transmit processor that processes data streams for output to the data stream output, and

data structures that are shared by the control data processor, the receive processor and/or the transmit processor and that contain information used by the receive processor and/or the transmit processor and the control data processor to coordinate pipelined processing of a data stream by the receive processor and/or the transmit processor and the control data processor.

8. An integrated circuit comprising:

a plurality of data stream inputs and/or outputs that receive and/or transmit data streams;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output and including

a receive processor that serially processes data streams received from the data stream input and/or

a transmit processor that serially processes data streams for output to the data stream output,

the receive processor and/or the transmit processor having a plurality of processing components and being configurable to bypass one or more of the components in processing the data streams.

9. An integrated circuit comprising:

a plurality of serial data stream inputs and/or outputs that receive and/or transmit data streams;

a plurality of data stream processors that process the data streams, each data stream processor being coupled to a data stream input and/or data stream output and including

a receive processor that serially processes data streams received from the serial data stream input and/or

a transmit processor that serially processes data streams for output to the serial data stream output,

the receive processor writing a processed data stream to a memory and/or the transmit processor reading a processed data stream from memory and the receive processor being reconfigurable to read a data stream to be processed from the memory and/or the transmit processor being reconfigurable to write a processed data stream to the memory.

10. An integrated circuit comprising:

a plurality of serial data stream inputs and/or outputs that serially receive and/or transmit data streams;

at least one set of parallel data stream inputs and/or outputs that receive and/or transmit data streams in parallel;

a plurality of serial data stream processors that process the data streams, each serial data stream processor being coupled to a serial data stream input and/or data stream output and including

a serial receive processor that processes data streams received from the serial data stream input and/or

a serial transmit processor that processes data streams for output to the data stream output; and

at least one parallel data stream processor that is coupled to the set of parallel data stream inputs, each parallel data stream processor including

a parallel receive processor that processes data streams received from the set of parallel data stream inputs, and/or

a parallel transmit processor that processes data streams for output to the set of parallel data stream inputs.

11. An integrated circuit comprising:

a plurality of I/O pins that receive and/or transmit signals;

a data stream processor that processes data represented by the signals;

a writeable configuration specifier for specifying a configuration of a plurality thereof; and

configuration circuitry coupled between the plurality of I/O pins and the data stream processor and responsive to the configuration specifier for configuring the I/O pins as specified by the configuration specifier,

whereby the integrated circuit may be used with a plurality of transmission protocols.

12. The integrated circuit set forth in claim 11 wherein:

the configuration specifier specifies electrical properties of the I/O pins; and

the configuration circuitry configures the I/O pins with the required electrical properties.

13. The integrated circuit set forth in claim 11 wherein:

there is a plurality of data stream processors; and

the configuration specifier specifies which of the plurality of data stream processors are connected to the plurality of I/O pins,

whereby a plurality of data stream processors may share processing of the data represented by the signals received and/or transmitted by the plurality of I/O pins.